1. A method of designing a hardware threaded circuit architecture, comprising:

determining a total area available for processing elements;

determining a set of task arrival times for tasks to be processed by the processing elements;

determining a number of possible implementations for the processing elements within the area available, each of the possible implementations having a corresponding number of processing elements;

interconnecting first and second ones of the processing elements;

determining overall system wait times for the possible implementations; and

selecting a first one of the possible implementations based upon the overall system wait times.

2. The method according to claim 1, further including determining an average steady state time the tasks spend in queue and/or an average steady state time the tasks spend in the processing elements.

3. The method according to claim 1, further including scheduling utilization of the processing elements to process the tasks.

4. The method according to claim 1, further including determining a number of the processing elements to be interconnected together in a hardware threaded arrangement.

5. The method according to claim 1, further including determining a state-based flow for an application to be processed by the circuit.

6. The method according to claim 6, further including determining a number of pipeline stages based upon the state-based flow for the application.

7. The method according to claim 6, further including generating a threaded schedule that can include parallel processing of the pipeline stages by at least two of the processing elements.

8. The method according to claim 7, further including reducing a frequency of operation and meeting a predetermined an overall system wait time.

9. The method according to claim 8, wherein the predetermined overall system wait time corresponds to an overall system wait time associated with non-threaded processing.

10. The method according to claim 7, further including reducing a supply voltage level while maintaining a predetermined overall system wait time.

11. The method according to claim 10, wherein the predetermined overall system wait time corresponds to an overall system wait time associated with non-threaded processing.

12. A circuit designed in accordance with claim 1.

13. A method of scheduling processing in a hardware threaded circuit, comprising:

receiving inputs corresponding to unthreaded processing of an application;

receiving information including processing element resources, a number of processing elements, and a window size corresponding to a number of downstream processing states to be examined; and

generating a hardware threaded schedule for processing the application with at least first and second one of the processing elements being interconnected to enable dynamic resource sharing.

14. The method according to claim 13, further including synthesizing the hardware threaded schedule to an Application Specific Circuit (ASC).

15. The method according to claim 14, further including synthesizing the hardware schedule to maximize throughput.

16. The method according to claim 14, further including synthesizing the hardware threaded schedule to reduce power consumption.

17. The method according to claim 13, further including receiving resource constraint information for the processing elements.

18. A hardware threaded circuit system, comprising:

a memory;

a task manager coupled to the memory; and

a plurality of processing elements coupled to the task manager, wherein first and second ones of the plurality of processing elements are interconnected for hardware threaded processing to enable dynamic borrowing of processing resources associated with the second one of the plurality of processing elements by the first one of the plurality of processing elements.

19. The system according to claim 18, wherein the circuit maximizes throughput.

20. The system according to claim 18, wherein the circuit reduces power consumption compared to a non-threaded processing for substantially similar system wait times.

21. The system according to claim 18, wherein the first and second processing elements each include a first type of resource and a second type of resource and a multiplexer such that the interconnection includes at least one input signal being provided to the first type of resource in the first and second processing elements.

22. The system according to claim 21, wherein the interconnection includes a connection from an output of the second processing element first type of resource to the first processing element.